What is claimed is:

1. A transistor device comprising:

a series of layers formed on a substrate, said layers including a first set of one or more layers each comprising n-type dopant material, a second set of layers forming a p-type modulation doped quantum well structure, and a third set of one or more layers each comprising n-type dopant material, wherein said first set of layers includes an n-type ohmic contact layer;

a collector terminal metal layer that is formed on one layer of said third set;

a plurality of p-type ion implant regions that are disposed on opposite sides of said collector terminal metal layer, said p-type ion implant regions operably coupled to said p-type modulation doped quantum well structure;

a patterned base terminal metal layer that is formed on said p-type ion implant regions for contact to said p-type modulation doped quantum well structure; and

a patterned emitter terminal metal layer that is formed on said n-type ohmic contact layer on said opposite sides of said collector terminal metal layer;

wherein said patterned base terminal metal layer is interdigitated with respect to said patterned emitter terminal layer on both of said opposite sides of said collector terminal metal layer.

2. A transistor device according to claim 1, further comprising:

a first capping layer that is formed above said collector terminal metal layer.

3. A transistor device according to claim 2, wherein:

said first capping layer comprises a silicon nitride film.

4. A transistor device according to claim 1, further comprising:

a top mesa upon which is formed said collector metal layer, a plurality of first mesas upon which is formed said patterned base terminal metal layer, and a plurality of second mesas upon which is formed said patterned emitter terminal metal layer; and

a second capping layer that covers sidewalls that extend from said plurality of first mesas to said top mesa as well as sidewalls that extend from said plurality of second mesas to said top mesa.

5. A transistor device according to claim 4, wherein:

said second capping layer covers said plurality of first mesas and said plurality of second mesas prior to metallization that forms said patterned base terminal metal layer and said patterned emitter terminal metal layer.

6. A transistor device according to claim 4, wherein:

at least one of said a collector terminal metal layer, said base terminal metal layer, and said emitter terminal metal layer are formed from a composite metal structure that is transformed into a low resistance metal layer by a rapid-thermal anneal operation.

7. A transistor device according to claim 6, wherein:

at least said base terminal metal layer and said emitter terminal metal layer are formed by deposition of a common composite metal structure.

8. A transistor device according to claim 6, wherein:

said composite metal structure protects against out diffusion of implanted ion species during the rapid thermal anneal operation.

9. A transistor device according to claim 6, wherein:

said low resistance metal layer is patterned with an etchant that selectively etches away portions of the composite metal structure that overlie said second capping layer.

10. A transistor device according to claim 6, wherein:

said composite metal structure comprises a multilayer sandwich that includes Nickel (Ni), Indium (In) and Tungsten (W) metals.

11. A transistor device according to claim 1, wherein:

said first set and second set of layers comprise epitaxial layers.

12. A transistor device according to claim 11, wherein:

said epitaxial layers are formed by molecular beam epitaxy.

13. A transistor device according to claim 1, wherein:

said third set of one or more layers is formed by ion implantation of n-type ions into a plurality of epitaxial layers.

14. A transistor device according to claim 13, wherein:

said plurality of epitaxial layers comprise a plurality of p-type layers.

15. A transistor device according to claim 13, wherein:

said plurality of epitaxial layers comprise at least one layer of an n-type modulation doped quantum well structure.

16. A transistor device according to claim 1, further comprising:

at least one undoped spacer layer disposed between said first set and said second set of layers; and

at least one undoped spacer layer disposed between said second set and said third set of layers.

17. A transistor device according to claim 1, wherein:

said second set of layers comprise at least one layer of undoped InGaAsN and at least one layer of undoped GaAs that form at least one quantum well.

18. A transistor device according to claim 1, wherein:

said second set of layers comprise at least one layer of AlGaAs of high p-type doping concentration to form a modulation doped layer for said at least one quantum well.

19. A transistor device according to claim 1, wherein:

said series of layers comprises group III-V materials.

20. A transistor device according to claim 1, wherein:

said series of layers comprises strained silicon heterostructures employing silicon-germanium (SiGe) layers.

21. A method of fabricating a transistor device comprising:

providing a series of layers formed on a substrate, said layers including a first set of one or more layers each comprising n-type dopant material, a second set of layers forming a p-type modulation doped quantum well structure, and a third set of one or more layers each comprising n-type dopant material, wherein said first set of layers includes an n-type ohmic contact layer;

depositing and patterning a collector terminal metal layer on one layer of said third set;

performing an etching operation that exposes a plurality of first mesas that are disposed on opposite sides of said collector terminal metal layer, and performing an ion implant of p-type ions through said first mesas to form a plurality of p-type ion implant regions that are disposed on said opposite sides of said collector terminal metal layer, said p-type ion implant regions operably coupled to said p-type modulation doped quantum well structure;

performing an etching operation that exposes a plurality of second mesas at said n-type ohmic contact layer that are disposed on said opposite sides of said collector terminal metal layer;

depositing and patterning a base terminal metal layer on portions of said first mesas, said portions being part of said p-type ion implant regions; and

depositing and patterning an emitter terminal metal layer on portions of said mesas at said n-type ohmic contact layer;

wherein said base terminal metal layer is interdigitated with respect to said emitter terminal metal layer on both of said opposite sides of said collector terminal metal layer.

22. A method of fabricating a transistor device according to claim 21, further comprising:

forming a first capping layer above said collector terminal metal layer.

23. A method of fabricating a transistor device according to claim 22, wherein:

said first capping layer comprises a nitride film.

24. A method of fabricating a transistor device according to claim 21, wherein:

said collector terminal metal layer is formed upon a top mesa, and a second capping layer is formed such that it covers sidewalls that extend from said first mesas to said top mesa as well as sidewalls that extend from said second mesas to said top mesa.

25. A method of fabricating a transistor device according to claim 24, wherein:

said second capping layer covers said plurality of first mesas and said plurality of second mesas prior to metallization that forms said base terminal metal layer and said emitter terminal metal layer.

26. A method of fabricating a transistor device according to claim 24, wherein:

at least one of said a collector terminal metal layer, said base terminal metal layer, and said emitter terminal metal layer are formed from a composite metal structure that is transformed into a low resistance metal layer by a rapid-thermal anneal operation.

27. A method of fabricating a transistor device according to claim 26, wherein:

at least said base terminal metal layer and said emitter terminal metal layer are formed by deposition of a common composite metal structure.

28. A method of fabricating a transistor device according to claim 26, wherein:

said composite metal structure protects against out diffusion of implanted ion species during the rapid thermal anneal operation.

29. A method of fabricating a transistor device according to claim 26, wherein:

said low resistance metal layer is patterned with an etchant that selectively etches away portions of the composite metal structure that overlie said second capping layer.

30. A method of fabricating a transistor device according to claim 26, wherein:

said composite metal structure comprises a multilayer sandwich that includes Nickel (Ni), Indium (In) and Tungsten (W) metals.

31. A method of fabricating a transistor device according to claim 21, wherein:

said first set and second set of layers comprise epitaxial layers.

32. A method of fabricating a transistor device according to claim 31, wherein:

said epitaxial layers are formed by molecular beam epitaxy.

33. A method of fabricating a transistor device according to claim 21, wherein:

said third set of one or more layers is formed by ion implantation of n-type ions into a plurality of epitaxial layers.

34. A method of fabricating a transistor device according to claim 33, wherein:

said plurality of epitaxial layers comprise a plurality of p-type layers.

35. A method of fabricating a transistor device according to claim 33, wherein:

said plurality of epitaxial layers comprise at least one layer of an n-type modulation doped quantum well structure.

36. A method of fabricating a transistor device according to claim 21, wherein:

at least one undoped spacer layer disposed between said first set and said second set of layers; and

at least one undoped spacer layer disposed between said second set and said third set of layers.

37. A method of fabricating a transistor device according to claim 21, wherein:

said second set of layers comprise at least one layer of undoped InGaAsN and at least one layer of undoped GaAs that form at least one quantum well.

38. A method of fabricating a transistor device according to claim 21, wherein:

said second set of layers comprise at least one layer of AlGaAs of high p-type doping concentration to form a modulation doped layer for said at least one quantum well.

39. A method of fabricating a transistor device according to claim 21, wherein:

said series of layers comprises group III-V materials.

40. A method of fabricating a transistor device according to claim 21, wherein:

said series of layers comprises strained silicon heterostructures employing silicon-germanium (SiGe) layers.